

### **Amendments to the Claims**

This listing of claims will replace all prior versions, and listings of claims in the application:

#### **Listing of Claims:**

Claim 1 (Previously Presented): An LSI device comprising:

an SOI substrate having an SOI layer including a core region to which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied;

a device separation region for separating the SOI layer into the core region and the interface region, wherein a thickness of the SOI layer of the core region is thinner than a thickness of the SOI layer of the interface region;

a plurality of first MOSFETs formed in the core region and in which the SOI layer of the core region is a fully depleted Si channel; and

a plurality of second MOSFETs formed in the interface region and in which the SOI layer of the interface region is a fully depleted Si channel,

wherein the first driving voltage is 1.5v and the second driving voltage is 3.3v.

Claim 2 (Previously Presented): An LSI device comprising:

an SOI substrate having an SOI layer including a core region to which a first driving voltage is applied and an interface region to which a second driving voltage

higher than the first driving voltage is applied;

a device separation region for separating the SOI layer into the core region and the interface region, wherein a thickness of the SOI layer of the core region is thinner than a thickness of the SOI layer of the interface region;

a plurality of first MOSFETs formed in the core region and in which the SOI layer of the core region is a fully depleted Si channel; and

a plurality of second MOSFETs formed in the interface region and in which the SOI layer of the interface region is a fully depleted Si channel,

wherein a channel length of the first MOSFETs formed in the core region are shorter than a channel length of the second MOSFETs formed in the interface region.

Claim 3 (Previously Presented): The LSI device according to claim 1, wherein a thickness of the SOI layer of the core region is 30nm or less.

Claim 4 (Previously Presented): The LSI device according to claim 3, wherein a thickness of the SOI layer of the interface region is around 50nm.

Claim 5 (Canceled)

Claim 6 (Canceled)

Claim 7 (Currently Amended): An [[The]] LSI device according to claim 6 comprising:

an SOI substrate having an SOI layer including a high speed computing region to which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied;

a device separation region for separating the SOI layer into the high speed computing region and the interface region, wherein a thickness of the SOI layer of the high speed computing region is thinner than a thickness of the SOI layer of the interface region;

a plurality of first MOSFETs formed in the high speed computing region and in which the SOI layer of the high speed computing region is a fully depleted Si channel;  
and

a plurality of second MOSFETs formed in the interface region and in which the SOI layer of the interface region is a fully depleted Si channel,

wherein a channel length of the first MOSFETs formed in the high speed computing region are shorter than a channel length of the second MOSFETs formed in the interface region.

Claims 8-9 (Canceled)

Claim 10 (Previously Presented): An [[The]] LSI device according to claim 6 comprising:

an SOI substrate having an SOI layer including a high speed computing region to

which a first driving voltage is applied and an interface region to which a second driving voltage higher than the first driving voltage is applied;

a device separation region for separating the SOI layer into the high speed computing region and the interface region, wherein a thickness of the SOI layer of the high speed computing region is thinner than a thickness of the SOI layer of the interface region;

a plurality of first MOSFETs formed in the high speed computing region and in which the SOI layer of the high speed computing region is a fully depleted Si channel;  
and

a plurality of second MOSFETs formed in the interface region and in which the SOI layer of the interface region is a fully depleted Si channel,

wherein the first driving voltage is 1.5v and the second driving voltage is 3.3v.